

ATTORNEY DOCKET: CPAC 1017.3

ELECTRONICALLY FILED ON 08 JANUARY 2007

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Marcos Karnezos

Application No.: 10/632,568

Filed: 02 August 2003

Title: SEMICONDUCTOR MULTI-PACKAGE MODULE HAVING PACKAGE STACKED OVER BALL GRID ARRAY PACKAGE AND HAVING WIRE BOND INTERCONNECT BETWEEN STACKED PACKAGES

Attorney Docket No.: CPAC 1017-3

Examiner: Douglas M. Menz

Group: 2891

Confirmation No.: 2603

Customer No. 22470

Box Issue Fee

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUBMISSION OF PRIOR ART AFTER NOTICE OF ALLOWANCE

Sir:

Applicants submit the below-listed documents to be placed in the file:

- Lee, U.S. Patent No. 5,652,185 issued 29 July 1997 for “Maximized Substrate Design for Grid Array Based Assemblies”.
- Nguyen et al., U. S. Patent No. 6,238,949 issued 29 May 2001 for “Method and Apparatus for Forming a Plastic Chip on a Chip Package Module”.
- Chen et al., U.S. Patent No. 6,441,496 issued 27 August 2002 for “Structure of Stacked Integrated Circuits”.
- Ishii et al., U.S. Patent No. 6,445,064 issued 03 September 2002 for “Semiconductor Device”.
- Pu et al., U.S. Patent No. 6,593,662 issued 15 July 2003 for “Stacked-Die Package Structure”.

- Glenn et al., U.S. Patent 6,650,019 issued 18 November 2003 for “Method of Making a Semiconductor Package Including Stacked Semiconductor Dies”.
- Uchida, U.S. Patent No. 6,690,089 issued 10 February 2004 for “Semiconductor Device Having Multi-Chip Package”.
- Koopmans, U.S. Patent 6,847,105 issued 25 January 2005 for “Bumping Technology in Stacked Die Configurations”.
- Kurita et al., U.S. Patent 6,930,396 issued 16 August 2005 for “Semiconductor Device and Method for Manufacturing the Same.”
- Karnezos, U.S. Patent No. 7,101,731 issued 5 September 2006 for “Semiconductor Multi-Package Module Having Inverted Second Package Stacked over Die-Up Flip-Chip Ball Grid Array (BGA) Package”.
- Fukui et al., U.S. Patent Publication No. 2002/0096755 published 25 July 2002 for “Semiconductor Device”.
- Wang, U.S. Patent Publication No. 2004/0212096 published 28 October 2004 for “Multi-Chips Stacked Package”.
- Su et al., U.S. Patent Publication No. 2006/0043556 published 02 March 2006 for “Stacked Packaging Methods and Structures”.

Respectfully submitted,

Date: 08 January 2007

/BILL KENNEDY/

Bill Kennedy, Reg. No. 33,407

HAYNES BEFFEL & WOLFELD LLP
P.O. Box 366
Half Moon Bay, CA 94019
(650) 712-0340 (telephone)
(650) 712-0263 (facsimile)